AMENDMENTS TO THE CLAIMS

Please amend claim 4 in accordance with the following list of the claims.

1. (Previously Presented) A digital switching system, comprising:

multiplexing means for multiplexing time slots from a first plurality of circuits;

switching memory means for storing and switching data of the time slots from the multiplexing means, for one frame period;

switching control means including a switching correspondence means for directing interchange of the time slots stored in the switching memory means in response to a switching request from a network received through an upper layer controller; and

demultiplexing means for demultiplexing into a second plurality of circuits, time slot data read out of the switching memory means using as addresses data from the switching correspondence means,

the switching correspondence means comprising:

information receiving means for receiving connection information from the upper layer controller;

read-out controlling means for storing the connection information corresponding to before or after switching, received through the information receiving means, to addresses designated by the connection information in one of a first memory means and a second memory means, and for sequentially reading out the stored connection information in read-out order of the switching memory means;

network switching control means for generating a switching signal in synchronization with an internal timing standard in response to the switching request provided by the upper layer controller; and

read-out selection means for selecting read-out from one of the first memory means and the second memory means of the read-out controlling means in response to the switching signal provided by the network switching control means.

2. (Previously Presented) A digital switching system according to claim 1, wherein with respect to the read-out controlling means, the first memory means and the second memory means are capable of independently and simultaneously writing and reading.

3. (Previously Presented) A digital switching system according to claim 1, wherein the network switching control means generates the switching signal to coincide with a beginning of a frame.

4. (Currently Amended) A digital switching system, comprising:

multiplexing means for multiplexing time slots from a first plurality of circuits;

switching memory means for storing and switching data of the time slots from the multiplexing means, for one frame period;

switching control means including a switching correspondence means for directing interchange of the time slots stored in the switching memory means in response to a switching request from a network received through an upper layer controller; and

demultiplexing means for demultiplexing into a second plurality of circuits, time slot data read out of the switching memory means using as addresses data from the switching correspondence means,

wherein the switching correspondence means comprises:

information receiving means for receiving connection information corresponding to before or after switching from the upper layer controller;

network switching control means for generating a switching signal in synchronization with an internal timing standard in response to the switching request provided by the upper layer controller;

working memory means for storing the connection information from the information receiving means, the working memory means reading out as a read-out signal the stored connection information in response to the switching signal from the network switching control means;

read-out selection means for selecting the connection information from one of the ~~switching~~ working memory means and the information receiving means, and outputting

the selected connection information in response to the switching signal from the network switching control means; and

read-out controlling means for storing the connection data outputted by the readout selection means, and for sequentially reading out the stored connection information in read-out order of the switching memory means.

5. (Previously Presented) A method of switching data in a digital switching system, comprising:

a multiplexing step of multiplexing time slots from a first plurality of circuits;

a writing step of sequentially writing into a switching memory data of the time slots multiplexed by the multiplexing step;

a data interchange step comprising receiving connection information from an upper layer controller, corresponding to before and after switching, writing the connection information in a control memory at addresses designated by the connection information, sequentially reading out the connection information stored in the control memory as read-out order for the multiplexed time slot data written in the switching memory, in synchronization with an internal timing standard in response to a switching directive from the upper layer controller, so as to change accommodation destinations of the multiplexed time slot data; and

a demultiplexing step of demultiplexing the data from the data interchange step into a second plurality of circuits.

6. (Previously Presented) A method of switching data in a digital switching system according to claim 5, wherein the data interchange step comprises:

an information receiving step of receiving the connection information from the upper layer controller before switching, and the same after switching, respectively;

an information input/output step of storing the connection information received in the information receiving step, and reading out the connection information received before and after switching;

a switching signal generation step of generating a switching signal for switching in synchronization with the timing in response to the switching directive of the connection information received from the upper layer controller;

a selection step of selecting the connection information after switching all of the connection information as read out in the information input/output step in response to the switching signal generated; and

a read-out step of reading out the multiplexed data as written in the writing step on the basis of the connection information selected in the selection step.

7. (Previously Presented) A method of switching data in a digital switching system according to claim 5, wherein the data interchange step comprises:

an information receiving step of receiving the connection information supplied from the upper layer controller before switching, and the same after switching, respectively;

an information writing step of writing the connection information for use after switching all of the connection information received in the information receiving step, when a switching request is delivered from the side of the upper layer;

a switching signal generation step of generating a switching signal for switching in synchronization with the timing in response to the switching directive of the connection information received from the upper layer controller;

a copying step of reading out the connection information after switching on a rising edge of the switching signal generated in the switching signal generation step as the connection information before switching;

a read-out step of storing the connection information as read out in the copying step, and reading out the multiplexed data as written in the writing step on the basis of the connection information; and

a selection step of selecting the connection information in response to a fall of the switching signal generated.

8. (Previously Presented) A method of switching data in a digital switching system, according to claim 7, wherein the copying step reads out addresses and data contained in

the connection information written in the information writing step, in increasing address order, supplying the same to the read-out step, and the read-out step writes data of connection information, as supplied, to an address indicated by the connection information, as supplied, while reading out the data written in increasing address order; and using the data as read-out addresses for the data of the time slots written in the writing step.